

Information Leakage Between FPGA Long Wires

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Abstract

As the capacity of FPGAs grows, it is becoming increasingly common for designers to incorporate IP from a range of third-party sources. The monolithic nature of FPGAs means that user circuits and black-box IP must share common infrastructure, such as routing resources. This physical proximity makes it easier for some cores to unintentionally leak secret data and for others to maliciously receive this information, even when there is no logical routing connection between them.

In this paper, we present a previously unexplored source of information leakage that occurs between adjacent but unconnected long wire segments. We find that wires carrying a logical 1 reduce the delay of nearby wires and this effect compounds linearly with the length and number of wires used. In contrast to previous research, which focuses primarily on detecting dynamic signals driven by large redundant circuits using external equipment, our work shows that the effect is measurable for small static and relatively short-lived signals, and that it can be detected using small onboard circuits. We are able to correctly infer the value driven onto the long wire over 95% of the time for signals that are anywhere from completely static to maintained for as little as $82\mu s$.

We show that the phenomenon is independent of location, can be replicated on different devices, and is measurable even when multiple competing circuits are present. Though we primarily conduct experiments on Virtex 5 devices, additional experiments on Virtex 4 and Virtex 6 FPGAs show that the phenomenon occurs across device generations.

1 Introduction

The ever-increasing size and sophistication of FPGAs make them an ideal platform for high-scale System-on-Chip integration. That said, this intrinsic sharing of the

reconfigurable fabric also means that many different cores have the potential to affect each other, even when they are not directly connected to one another. This is because the operation of one circuit can cause subtle, yet measurable changes elsewhere on the device, through a variety of different mechanisms such as variations in power/ground voltage, capacitive or inductive coupling, etc.

Although potentially noisy, these effects can be used for side-channel communication. They can be leveraged intentionally, for example to implement a minimal-impact debugging tap or a no-contact watermark. These side-channel communication techniques also have important security implications if they cause information to leave an IP block unintentionally. For example, a core performing digital rights management likely contains sensitive encryption keys. Thus, it is critical to identify and characterize different mechanisms and implementations of these kinds of information leaks. Furthermore, testing on physical FPGAs will allow us to understand the limits and potential risk.

In this paper, we investigate a side-channel communication mechanism that, to the best of our knowledge, has not been previously documented: that the value driven onto a long line influences the delay of other nearby long lines. That is, if a long line carries a logical 1, the delay of nearby long lines will be slightly lower than when it carries a logical 0. To demonstrate this phenomenon we build a simple transmitter/receiver pair. The transmitter consists of a long wire connecting a source LUT and a sink LUT. The receiver consists of three LUTs connected to form a Ring Oscillator (RO), where one connection in the RO uses a long wire that is a neighbor of the transmitting long wire (Figure 1). When the transmitting long wire carries a logical 1, the routing delay around the RO decreases, which results in a small increase in the RO frequency. We detect these minor differences in RO frequency by counting the number of signal changes that occur per unit time.

We conduct extensive experiments on multiple Xilinx prototyping boards and show that the phenomenon is lo-

*Work conducted at Microsoft Research.

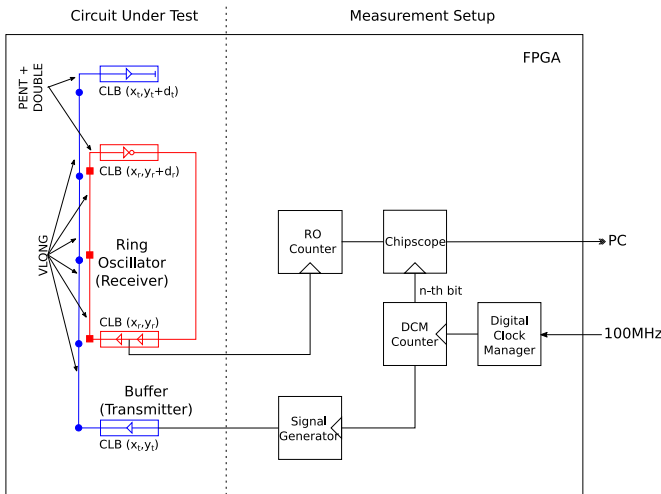


Figure 1: Block diagram of our setup

cation and device independent. We perform all tests in an uncontrolled physical environment and on stock prototyping boards (i.e., without modifications such as additional decoupling capacitors or improved voltage regulators). This indicates that the phenomenon can be detected even in the presence of environmental noise, which otherwise impacts RO frequency [4].

Although we perform a variety of different experiments to characterize the behavior of this side-channel communication, we do not attempt to determine the precise electrical mechanism that causes it. That is, we have determined attributes such as when the phenomenon occurs, how strong the effect is, and how we might reduce noise in the transmission, but we have not attempted to determine if this is caused by ground bounce, capacitive coupling, etc. This is for two reasons. First, we have demonstrated this behavior on commercial FPGAs and precisely determining the electrical cause would be very difficult without access to design information such as the physical layout and process-specific parameters. Second, end-users of such devices cannot change the physical design of the chips themselves. This is certainly true for existing devices already in the field and eliminating something such as localized power sag in new devices would likely require modifying the internal power distribution framework. Rather, end-users can only change the placement and routing of their circuits. Thus, characterization of the side-channel at this level is more pertinent.

2 Related work

Ring Oscillator frequencies depend on Process, Voltage, and Temperature (PVT) variations [4], and this dependence makes them suitable for a range of applications from temperature sensing [2, 15], to side-channel receivers [11, 13]. Consequently, any mechanism which can

be used to manipulate the frequency of ROs can also be used to attack these applications. For instance, since ROs are used as True Random Number Generators (TRNGs) and Physically Unclonable Functions (PUFs), influencing the delays of ROs by altering the power supply [7] or by injecting EM signals [1] can result in low entropy and cloneability.

One such mechanism that can affect the frequency of ROs is crosstalk [3], and delays and faults due to crosstalk can be estimated in a built-in or on-line fashion [12, 9]. A switching pattern which follows the RO increases the RO’s oscillation frequency by 1-9% compared to a pattern that opposes it, when the RO and transmitter circuits are in sync [3]. To achieve this synchronization, however, requires the transmitter to be connected to the output of one of the RO’s stages. As a result, as presented, this mechanism cannot be used directly for side-channel communication or to reliably attack the ring oscillator, due to the high accuracy of prediction required for the frequency and phase of the oscillator.

Recently, more emphasis has been placed on using networks of ROs to detect Hardware Trojans on a device [5, 14]. The dynamic power consumed by HTs results in a voltage drop that lowers the RO frequencies compared to the Trojan-free “golden” IC, making them detectable. Our work is fundamentally different, not only because of the application domain, but because the phenomenon demonstrated decreases rather than increases RO delay and frequency. Moreover, we demonstrate this phenomenon over both static and relatively slowly changing signals. Prior work [10] has shown that static and slowly changing signals can be much more difficult to detect, requiring either very large circuits (over 14k registers) or long measurement times (2.5h), external measurement equipment, and special modifications to the device, including directly driving internal VDD pins, and turning off I/O and UART transmissions.

By contrast, we can distinguish between the values of signals which remain constant (i.e., have no switching activity) during our period of measurement, which is as low as $82\mu s$. This measurement period is also a lower yet unrealized bound for on-chip HT detection using ROs [6]. Our transmitter and receiver circuits can be implemented with a small handful of LUTs and wire segments, and measurements do not need external equipment or additional control over voltage or temperature conditions.

3 Overview

In this section we describe two simple experiments, briefly demonstrating the observed phenomenon. By contrasting the two results, we motivate the choices we make for our experimental setup and the parameters that we control and test. These tests are described in greater detail in Section 4.

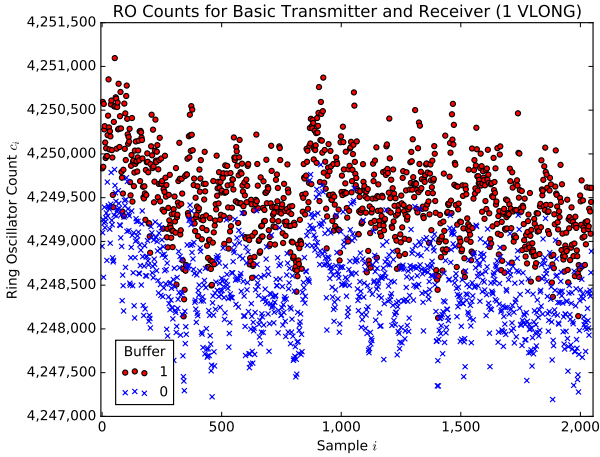


Figure 2: RO counts for basic setup (1 VLONG)

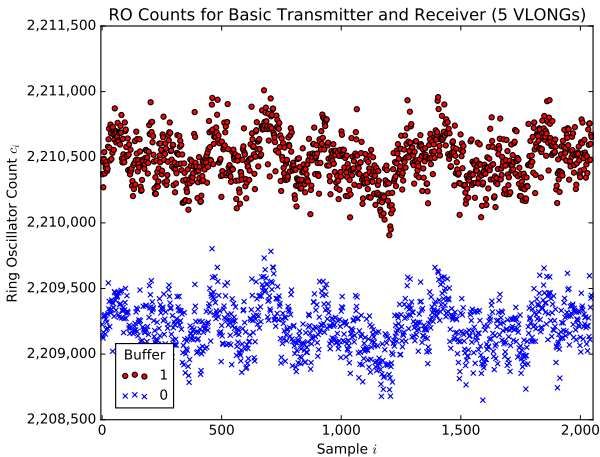


Figure 3: RO counts for basic setup (5 VLONGs)

In the most basic setup, as shown in Figure 1, we have a *transmitting* circuit, shown in blue, which consists of a long vertical wire, and is driven by a buffer LUT (the output mirrors the input). The long wire consists of one or more consecutive VLONG segments, denoted with blue dots. This connection terminates at another buffer LUT, the output of which is left unconnected, to minimize the amount of resources used. The *receiving* circuit, shown in red, is a three-stage ring oscillator. One of the RO connections uses VLONGs (red squares) that are adjacent to the transmitter’s wire segments (i.e., in the same routing channel). The ring oscillator is connected to a counter, and every 2^{21} ticks of a 100MHz clock (21ms), the counter is sampled and reset. At each reset of the counter, the signal driving the transmitting circuit toggles from 0 to 1, or vice versa.

In the first test, both circuits use one VLONG each. Figure 2 shows the ring oscillator counts c_i on a Virtex 5

| #VLONGs | μ_0 | σ_0 | μ_1 | σ_1 | $\Delta\mu$ |
|---------|-----------|------------|-----------|------------|-------------|
| 1 | 4,248,485 | 471 | 4,249,491 | 476 | 1,006 |
| 5 | 2,209,208 | 182 | 2,210,482 | 177 | 1,274 |

Table 1: Means μ and std. deviations σ for the two setups

device for 2048 sampling periods (roughly 44 seconds). The ring oscillator counts when the transmitter carries a 1 (red dots) are relatively higher than the counts for a 0 (blue X’s), though the overall ring oscillator frequency drifts over time, likely due to variations in environmental conditions. Figure 3 then repeats this experiment, but for circuits which use 5 VLONGs. We notice that the phenomenon is much more pronounced compared to the previous experiment, and the pattern is clearly distinguishable even despite local fluctuations. The mean and standard deviations of the RO counts for the two tests are shown in Table 1.

4 Experimental Setup

In order to characterize the phenomenon more precisely, we need to identify the factors we wish to vary and test, keeping the rest of the setup fixed. Briefly, we show that the phenomenon does not depend on factors such as the device used and the location of the circuits on the device, while it is heavily affected by factors such as the number of VLONGs used and the duration of transmission.

As shown in Figure 1, our experimental setup can be divided into two sets of components. The first is the Circuit Under Test (CUT), consisting of both the transmitter and receiver, whose parameters we vary. The second is the measurement component, which works independently of the specific CUT and generates the transmitted signal, samples the RO counter, and transfers this data to a PC for analysis.

4.1 Measurement Setup

Sample triggering for the measurement component occurs every $N = 2^n$ clock ticks and is implemented with a counter. The system uses a 100MHz clock, driven by a Digital Clock Manager (DCM) to ensure clock quality. At every trigger event, the RO counter is read and reset, and, unless stated otherwise, this is the only time a new value is presented to the transmitter. For the majority of our experiments, we use $n = 21$ (21ms), but vary n in Section 5.4. The sampled data is transferred to a PC for analysis through ChipScope’s Integrated Logic Analyzer (ILA). No other I/O is used.

The bulk of our experiments are conducted on three XUPV5-LX110T evaluations boards, which contain a XC5VLX110T Virtex 5 chip in a 35x35mm FF1136 package. The boards include a heatsink and a fan, but we

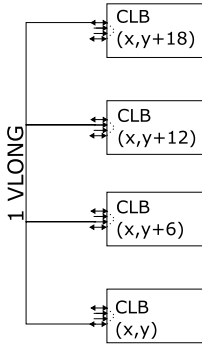


Figure 4: VLONG connections for CLB (x, y)

do not otherwise control for temperature. Two of the boards are powered by the factory-provided 5V power supplies, while one board is powered through an Agilent E3610A benchtop power supply. Thus, while the benchtop supply provides slightly more stable power to one of the boards, all three devices still rely on the factory board-level voltage regulators. We collect data for over 100 setup configurations spread over 10 experiments, varying the placement, length, and transmission patterns of the CUT. Each is run on every device 5 times, collecting 2048 data points per run, for approximately 10 hours of measurements per device.

We use Xilinx’s ISE Design Suite 14.6 for synthesizing, mapping, and routing, and we add KEEP and SAVE NET constraints to ensure that our logic is not optimized or renamed. Unlike the CUT described below, the measurement logic is not hand-placed or hand-routed, due to the large number of experiments performed. Although the measurement logic could influence the RO frequency [8], we repeat our experiments on multiple locations, control for other patterns, and average over relatively lengthy periods of time. Thus, we believe that any effects of the measurement circuitry influences the transmission of both zeros and ones equally.

4.2 Circuit Under Test

The transmitter and receiver are hard-macros created with FPGA Editor and are placed at specific locations using the LOC constraint. To more easily describe the layout, we briefly describe the Virtex 5 architecture.

Every Virtex 5 Configurable Logic Block (CLB) can be identified by an (x, y) coordinate on the chip and consists of two slices, each with four LUT6 6-input Look Up Tables (LUT). These LUTs are named A through D. The routing between different elements within a CLB or between CLBs goes through a component called a *switch matrix*. There are multiple types of routing wires, but we are primarily interested in vertical LONGs (VLONGs). As will be discussed later, the phenomenon can also be observed with horizontal long wires (HLONGs).

Figure 4 shows the CLBs that can access any given VLONG. A VLONG runs the length of 18 CLBs and has 4 taps, evenly spaced 6 CLBs apart. However, only the first and last taps can drive the wire, with the other two only being used as outputs. At the end of each VLONGs there is a (programmable) connection that allows the chaining of multiple VLONGs together. To use a VLONG output as an input to an LUT, the signal must first go through a PENT and then a DOUBLE wire. As a result, the total distance separating 2 CLBs using v VLONGs (of total length l) is $d = 18v + 3 + 1 = l + 4$.

As mentioned earlier, the transmitter signal passes through an LUT which buffers its input, travels through the VLONGs, and terminates at an otherwise unconnected buffer LUT. The ROs are set up in a similar fashion, such that one connection in the ring uses VLONGs. The signal at the bottom CLB passes through two LUT buffers, while the signal at the top CLB is inverted and then routed back to the input of the bottom CLB.

5 Experimental Results

In this section, we present the results of our experiments. We start in Section 5.1 by discussing techniques for classifying the measured data, and introduce notation and metrics to estimate the effect of the phenomenon in Section 5.2.

Section 5.3 then investigates the effect of the relative placement between the transmitter and the receiver and their absolute location on the device. Briefly, we find that the phenomenon depends on the distance between the long wires, and not on the device used and the absolute placement.

Section 5.4 tests the influence of receiver measurement time. Although the relative effect remains the same irrespective of the duration of transmission, in absolute terms, longer measurement periods make the values easier to infer.

Section 5.5 examines the effect of transmitter switching activity. We demonstrate that the phenomenon only depends on the currently transmitted value, and not on the values transmitted in the past. It also shows that the phenomenon we describe dominates an opposing effect caused by switching activity.

Section 5.6 illustrates the effect of longer overlaps between the transmitter and the receiver. We find that the longer the overlap, the more pronounced the effect is.

Section 5.7 reveals what occurs when there are multiple nearby transmitters. We demonstrate that the transmitted values can still be clearly distinguished from one another.

Finally, we briefly discuss some additional experiments in Section 5.8, including preliminary results that suggest that the behavior is also present in other Virtex generations.

| ID | l | t | c_i^1 | c_i^2 | c_i^4 |
|----|----|------------|---------|---------|---------|
| 0 | 6 | 21ms | 0.09 | 5.15 | 5.53 |
| 1 | 6 | 21ms | 0.01 | 1.26 | 1.54 |
| 2 | 6 | 21ms | 0.04 | 3.90 | 4.27 |
| 0 | 36 | 82 μ s | 0.25 | 4.58 | 3.96 |
| 1 | 36 | 82 μ s | 0.32 | 3.22 | 3.02 |
| 2 | 36 | 82 μ s | 0.94 | 3.55 | 3.55 |

Table 2: Threshold errors (%) for different devices, measurement times t and receiver and transmitter lengths l .

5.1 Predictions

The results presented in Section 3 show that the RO frequency drifts significantly, likely due to changes in environmental conditions, such as temperature and voltage variation. These tests also show that, at least in some cases, one cannot use a simple frequency threshold to classify the measured data. In this section, we propose a simple technique to infer transmitted ones versus zeros: a moving average.

Denoting the i -th sampled count with c_i , let

$$c_i^j = \frac{c_{i-1} + \dots + c_{i-j}}{j}$$

be the average of the previous j measurements. In our basic setup the transmitter alternates between sending ones and zeros,¹ so for even j this quantity averages a balanced number of zeros and ones while for odd j it is *biased*. That is, c_i contains an uneven number of samples for ones and zeros, raising or lowering the running average respectively.

As shown in Table 2, classifying the i -th measurement as a 1 when $c_i > c_i^j$ and a 0 otherwise results in low errors. We show the classification results for two completely different setups, tested on all three Virtex 5 devices. In the top half of Table 2 we use long measurement times ($n = 21$, or $t = 21$ ms) with a small VLONG overlap (the two circuits only share a portion of a VLONG since $l = 6$, see Figure 4). In the bottom half of Table 2 we use short measurement times ($n = 13$, or $t = 82\mu$ s) but the transmitter and receiver overlap for 2 full VLONGs ($l = 36$).

Table 2 shows that a simple unbiased moving average (even j) has an accuracy between 94.5-98.5% across all measurements. When we use a biased average (odd j , in this case $j = 1$, so we are only comparing with the most recent value), the accuracy rises to 99.0-99.9%.

Also notice that, out of the three devices, we are able to infer the transmitted value with greater accuracy on device 1. We suspect this is because that is the device

¹In Section 5.5 we show that the behavior persists even under different patterns, but this alternation simplifies our discussion in this section.

connected to the benchtop power supply, which has better regulation and noise characteristics as compared to the low-cost factory-provided power bricks. This helps eliminate a source of environmental noise that makes observing our target phenomenon more difficult. When the device ID is not mentioned in future tests, we are using device 0, which is the noisiest of the three and presents worst-case results.

5.2 Counts and Frequency

Although useful for demonstrating the basics of the observed phenomenon, the very simplistic classification method described above is not general. For example, in most situations we will not have labelled data and the transmitted values may not have a balanced number of zeros and ones. That said, the broad issue of removing noise and modeling or classifying data is a well-established problem. As a result, we do not further address this aspect here. Rather, in the analyses in the following sections we utilize the fact that we know the transmitted value and instead focus on the changes in relative RO frequency that result.

We can estimate the relative changes in RO frequency based on the sampled counts because f_{RO}/f_{CLK} can be approximated by $c/2^n$ (within an appropriate quantization error due to the unsynchronized nature of the RO and the system clock). Thus,

$$\frac{f_{RO}^1 - f_{RO}^0}{f_{RO}^1} \approx \frac{C^1 - C^0}{C^1} \quad (1)$$

where C^i and f^i represent the count and respective frequency when the transmitter has value i .

In the basic setup, the transmitter alternates between zeros and ones. Thus, the pair $p_i = (c_i, c_{i-1})$ always corresponds to different transmitted values. For the sake of notation clarity, we will assume that c_{2i+1} corresponds to a transmitted 1 and we will use the quantity

$$R\Delta C_i = \frac{c_{2i+1} - c_{2i}}{c_{2i+1}}$$

to indicate the relative frequency change between a transmitted one and zero. $R\Delta C$ will denote the average of $R\Delta C_i$ over all pairs of measurements i . Unless specified otherwise, we average the results per device across five independent experimental runs.

5.3 Placement

In this section, we investigate the different aspects of receiver and transmitter placement, shown in Figure 5. The transmitter’s long wires are depicted with blue dots and the receiver’s with red squares. The transmitter has length l_t and the receiver l_r , each of which use $l_x/18$

| ID | (2, 1) | (6, 110) | (10, 1) | (34, 34) | (50, 84) | (58, 34) | (98, 1) | (102, 110) | (102, 14) | (106, 1) |
|----|--------|----------|---------|----------|----------|----------|---------|------------|-----------|----------|
| 0 | 3.554 | 3.476 | 3.423 | 3.559 | 3.605 | 3.495 | 3.523 | 3.406 | 3.533 | 3.603 |
| 1 | 3.108 | 3.155 | 3.184 | 3.162 | 3.235 | 3.228 | 3.281 | 3.180 | 3.275 | 3.164 |
| 2 | 3.504 | 3.462 | 3.444 | 3.465 | 3.713 | 3.589 | 3.675 | 3.565 | 3.673 | 3.650 |

Table 3: $R\Delta C \cdot 10^4$ for different devices and absolute CUT placements (x_r, y_r)

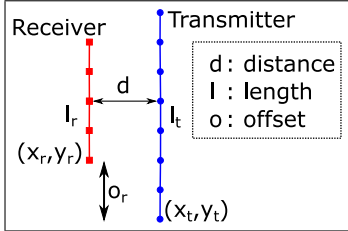


Figure 5: Relative placement of VLONGs for receiver (red squares) and transmitter (blue dots)

| ID | right | CV_r | left | CV_l |
|----|-------|--------|-------|--------|
| 0 | 3.532 | 0.176 | 3.753 | 0.170 |
| 1 | 3.124 | 0.189 | 3.381 | 0.171 |
| 2 | 3.583 | 0.180 | 3.757 | 0.203 |

Table 4: $R\Delta C \cdot 10^4$ and CV when the transmitter wires are to the right ($d = 1$) or left ($d = -1$) of the receiver wires

VLONG segments. For a fixed set of receiver and transmitter lengths we can change three independent parameters: the distance d between the wires (Section 5.3.1), the absolute (x, y) location where the entire CUT is placed (Section 5.3.2), and the relative location of overlap, determined by the relative offset o_r between the transmitter’s and receiver’s starting locations (Section 5.3.3). In Section 5.3.4 we also test if the direction of transmitter and receiver signal propagation (up vs. down) affects the results. Overall, we determine that only distance has a meaningful influence on the observed phenomenon.

5.3.1 Distance

Table 4 shows the effect when the transmitter uses the VLONG to the right ($d = 1$) or left ($d = -1$) of the receiver. For this test, we place the CUT at locations $(x_r, y_r) = (6, 14)$ and $(x_t, y_t) = (6, 14 \pm 1)$. The transmitter and receiver are not offset ($o_r = 0$) and both circuits use 2 VLONGs ($l = 36$). As shown, the relative change in frequency and coefficient of variation of the $R\Delta C$ (CV, defined as σ/μ) are quite similar, though the effect is slightly more pronounced for $d = -1$. The Kolmogorov-Smirnov test suggests that the data comes from different distributions with certainty ($p = 0$).

The effect remains statistically significant ($p < 10^{-6}$)

| ID | 0 | 18 | 36 | 54 |
|----|-------|-------|-------|-------|
| 0 | 3.517 | 3.434 | 3.557 | 3.617 |
| 1 | 3.122 | 2.994 | 3.042 | 3.236 |
| 2 | 3.557 | 3.354 | 3.451 | 3.695 |

Table 5: $R\Delta C \cdot 10^4$ for different relative offsets o_r

even when the distance is increased to $d = \pm 2$, but the effect is $20\times$ weaker, and the coefficient of variation is over 3.1. For distances beyond 2, the data is uncorrelated with $p > 0.75$.

5.3.2 Absolute Location

In this experiment, we continue to use $l = 36$ and $o_r = 0$, but we fix $d = -1$ and vary the absolute location of the CUT (x_r, y_r) and $(x_t, y_t) = (x_r, y_r - 1)$. The results are presented in Table 3. As shown, the resulting values are very similar, even though we do not control the placement and routing of measurement circuit due to the manual effort. As before, device 1 has smaller variability compared to the other devices. Note that the above locations use SLICEM resources (which contain distributed RAM), and hence $x = 2 \pmod 4$. Similar results are obtained for SLICEL resources, though the internal routing from the LUTs to the VLONG changes slightly.

5.3.3 Relative Start

In this experiment, we fix the transmitter at $(x_t, y_t) = (6, 13)$, the distance $d = -1$ and change the location of the transmitter and receiver overlap by changing o_r . In order for the distance between the transmitter and the receiver VLONGs to remain the same, o_r needs to be a multiple of the VLONG length ($= 18$). This is due to the routing restrictions imposed by the device that were discussed in Section 4.2. To offer multiple offset options, we set $l_r = 36$ and $l_t = 90$ (i.e., there are four possible arrangements where the transmitter and receiver overlap by 2 VLONGs). As shown in Table 5, again there is some variability among the different arrangements, but it is on the same order as that seen when changing the absolute location (Section 5.3.2).

| ID | ↑↑ | ↓↑ | ↑↓ | ↓↓ |
|----|-------|-------|-------|-------|
| 0 | 3.414 | 3.475 | 3.643 | 3.690 |
| 1 | 2.999 | 3.048 | 3.221 | 3.276 |
| 2 | 3.347 | 3.417 | 3.614 | 3.619 |

Table 6: $R\Delta C \cdot 10^4$ for different RO and buffer directions

| n | t | ΔC | $R\Delta C \cdot 10^4$ | CV |
|----|---------------|------------|------------------------|-------|
| 13 | 81.9 μ s | 4 | 3.553 | 0.343 |
| 15 | 327.7 μ s | 18 | 3.526 | 0.238 |
| 17 | 1.3ms | 75 | 3.526 | 0.198 |
| 19 | 5.2ms | 303 | 3.529 | 0.172 |
| 21 | 21.0ms | 1213 | 3.531 | 0.172 |
| 23 | 83.9ms | 4864 | 3.539 | 0.179 |

Table 7: Absolute and relative count differences and coeff. of variation for different measurement times on device 0

5.3.4 Direction

As in the previous experiment, we fix the bottom slice of the transmitter at $(x_t, y_t) = (6, 13)$, the lengths $l_r = 36$, $l_t = 90$, the distance $d = -1$, and the relative offset $o_r = 18$. We now vary the direction of the signal propagation for the transmitter and receiver VLONGs. In the previous experiments, both the transmitter and receiver signals travelled from the bottom of the device to the top. Table 6 shows the results for the 4 different direction configurations (receiver up/transmitter up, receiver down/transmitter up, etc.). As before, the variability in the results is similar to that seen when changing the absolute location (Section 5.3.2). Although the same transmitter and receiver VLONGs are used in these tests, this variability is to be expected. This is because the driver at the bottom of a VLONG is physically distinct from the driver at the top. Similarly, as discussed in Section 4.2, a PENT and a DOUBLE are needed to connect the output of a VLONG to the input of a CLB. Therefore, different PENTs and DOUBLES must be used at the respective top and bottom CLBs of the receiver and transmitter.

Over the course of these first four tests, we have found that the effects remain approximately constant for all parameter choices, with the exception of d . Thus, for the remaining experiments we arbitrarily fix $d = -1$, $l = 36$, $o_r = 0$, $(x_r, y_r) = (6, 14)$ and $(x_t, y_t) = (6, 13)$.

5.4 Measurement Time

In this section, we investigate the effect of measurement time on the quality of the received signal. Table 7 presents the average absolute count differences ΔC and relative count differences $R\Delta C$ for different measurement periods n . The buffer value is kept constant for 2^n

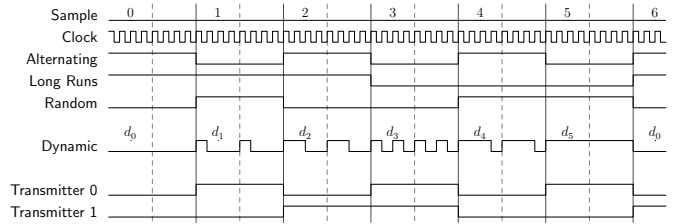


Figure 6: Timing diagram for the various transmission patterns

| ID | Alternating | Long Runs | Random |
|----|-------------|-----------|--------|
| 0 | 1216.9 | 1199.5 | 1214.8 |
| 1 | 1055.1 | 1030.9 | 1061.4 |
| 2 | 1202.5 | 1220.8 | 1207.0 |

Table 9: Average ΔC for various transmission patterns

100MHz clock ticks while the ring oscillator is counting. The data confirms the theoretical prediction of Equation 1, which suggests that $R\Delta C$ is approximately the same for all values of n . For this to be true, ΔC must grow linearly with increasing measurement time. This means that larger values of n increase the separation between the two counts, making it easier to detect the transmitted value. Moreover, a smaller n results in higher CV due to noise. However, there is always a persistent variation (about 17-18%) which cannot be removed, likely due to environmental factors. The coefficient of variation of the absolute count differences and of the relative count differences is the same to three significant digits, and is thus shown only once in the table. Based on these findings, we fix $n = 21$ for the remaining experiments.

5.5 Transmitter Patterns

In this set of experiments we show that the phenomenon does not fundamentally depend upon the slowly alternating pattern used thus far. We first show this for relatively constant signals (Section 5.5.1), and then for highly dynamic signals (Section 5.5.2). Finally, we compare this phenomenon to the effect of switching activity traditionally discussed for Hardware Trojan detection (Section 5.5.3).

5.5.1 Constant Signals

In this section, we describe two experiments to show that, for slowly changing signals, the phenomenon is solely dependent upon the values transmitted and not the pattern between consecutive values.

As shown in Figure 6, the previous experiments have all used a slowly alternating signal (*Alternating*). In this experiment, we sample the ring oscillator at the same rate as before ($n = 21$) while greatly slowing down the

| Transmitter Type | LUTs | Metric | $d_0 = 0000$ | $d_1 = 1000$ | $d_2 = 1100$ | $d_3 = 1010$ | $d_4 = 1110$ |
|---------------------------------------|---------|------------|--------------|--------------|--------------|--------------|--------------|
| Long Wires | 2 | Δ_i | 1197.3 | 882.2 | 589.2 | 580.8 | 282.8 |
| | | CV | 0.179 | 0.287 | 0.480 | 0.521 | 1.111 |
| Short Wires (LUTs next to RO CLBs) | 2 * 328 | Δ_i | 14.8 | 487.8 | 486.6 | 948.6 | 487.0 |
| | | CV | 15.369 | 0.603 | 0.657 | 0.343 | 0.727 |
| Short Wires (LUTs between RO CLBs) | 1 * 312 | Δ_i | 72.5 | 281.5 | 260.1 | 491.9 | 258.1 |
| | | CV | 2.794 | 0.950 | 1.162 | 0.666 | 1.289 |

Table 8: Effect of dynamic switching activity for different patterns and different transmitters

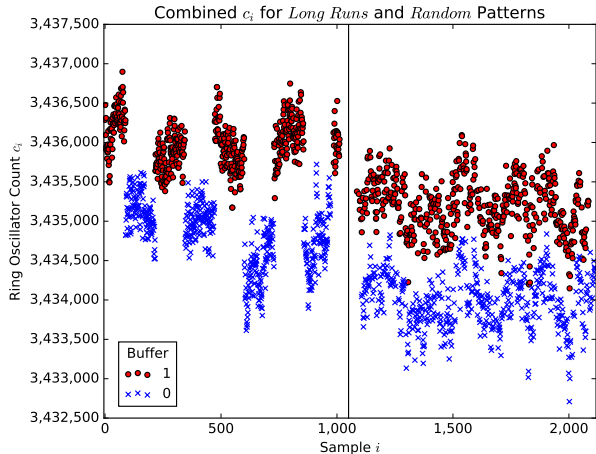


Figure 7: Constant patterns: Long Runs (left), Random (right)

alternation speed of the transmitted signal (*Long Runs*). Rather than switching the transmitted signal every sample period, we now maintain the same value for 128 consecutive triggers – in essence, testing the effects of long sequences of zeros and ones. The results of this test are shown in the left of Figure 7. In the second experiment we transmit a pseudo-random pattern of zeros and ones by connecting a Linear Feedback Shift Register (*Random*) to the transmitter. The results of this test are shown in the right of Figure 7.

In both experiments, the RO counter samples remain significantly higher when transmitting a one versus a zero. As shown in Table 9, the average ΔC for the alternating, long runs, and random transmissions are virtually identical. However, note that even though the three patterns behave similarly, the input is not guaranteed to have a balanced number of zeros and ones (locally for the long runs and neither locally nor globally for the LFSR). This presents a fundamentally different challenge for the classification discussed in Section 5.1.

5.5.2 Dynamic Patterns

In this experiment, we show that the dominating factor in the observed phenomenon is the duration for which the transmitter remains at a logical 1, and *not* the switching activity of the circuit. To that end, as shown in Figure 6 (*Dynamic*), during each sampling period we loop the transmitter quickly through a 4-bit pattern at 100MHz. We test six different 4-bit patterns, only updating the looped pattern in-between sampling periods. For example, for the pattern 1100, the transmitter would stay high for two 100 MHz clock ticks, then low for two clock tick, then back to high for 2 ticks, etc., until the end of the sampling period. This is shown as *Dynamic*, d_2 in Figure 6. The six 4-bit patterns used are: $d_0 = 0000$, $d_1 = 1000$, $d_2 = 1100$, $d_3 = 1010$, $d_4 = 1110$, and $d_5 = 1111$.

Notice that d_0 and d_5 are similar to the slowly changing transmissions used for the majority of test described earlier, but d_1 through d_4 are very quickly changing transmissions. Also notice that while d_1 , d_2 , and d_4 have the same switching activity (1 rising and 1 falling transition per 4 cycles), they transmit a one for different fractions of the sampling period (25, 50, and 75% respectively). Lastly, notice that while d_2 and d_3 transmit the same fraction of ones, d_3 has twice the switching activity (2 rising and 2 falling transitions per 4 cycles rather than 1 of each).

The top rows of Table 8 show the average count differences $\Delta_i = C_5 - C_i$ between d_5 (all ones) and all other patterns d_i , and the corresponding coefficient of variation. All Δ_i 's are positive, meaning that transmitting all ones results in the highest RO frequency. Furthermore, $\Delta_4 < \Delta_3 \approx \Delta_2 < \Delta_1 < \Delta_0$, which exactly mirrors the ordering of the patterns in terms of their one versus zero duty cycles (transmitting 75% ones has a higher frequency than transmitting 50% ones, etc.). This ordering and the fact that there is no significant difference between Δ_2 and Δ_3 supports our claim that the change in RO frequency is not affected by switching activity, but solely influenced by the amount of time that a one versus zero is transmitted.

As another note, the measurements for all pairs of patterns differ with a statistical significance of at least 10^{-10} according to the Kolmogorov-Smirnov test. The excep-

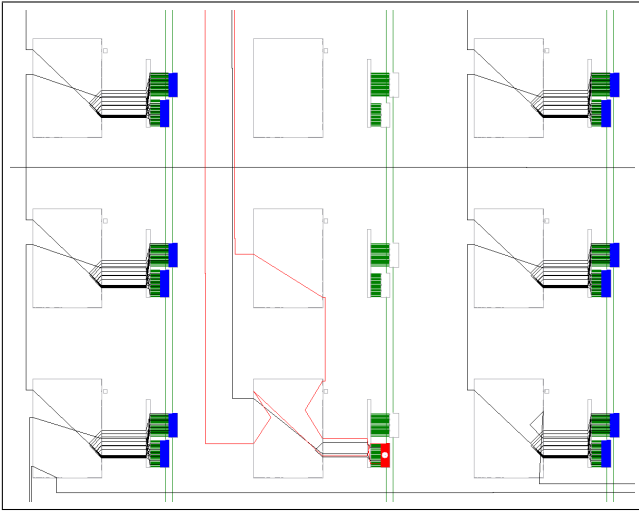


Figure 8: Start of two 328-stage buffers using packed local routing (blue) and ring oscillator macro (red)

tion are the patterns d_2 and d_3 , which both transmit a one for an equal amount of time, in which the distributions are the same ($p > 0.5$).

5.5.3 Local Routing

Previous research on Hardware Trojan detection [5, 14] has noted that high switching activity of a circuit can affect the frequency of nearby ring oscillators. However, these efforts have found a *decrease* in oscillation frequency, likely due to power sag or ground bounce, rather than the increase in oscillation frequency for the phenomenon reported here.

In this section, we show that we can replicate the phenomenon reported in earlier work - when the transmitter is large (i.e., uses multiple redundant buffers), generates a lot of switching activity, and does not share a long line with the receiver, the observed RO frequency is indeed reduced.

In this experiment, we construct a ring oscillator as before, using 2 VLONGs starting at $(x_r, y_r) = (6, 14)$, but we surround the ring oscillator with a large transmitter, consisting of a left and right vertical bank of 328 buffer stages over the span of the RO. This is partially shown in a screenshot from FPGA Editor (Figure 8). To ensure that the stages are placed appropriately and chained using intra-CLB routing, we programmatically generated BEL, RLOC, and RLOC_ORIGIN constraints.

Shown in the middle rows of Table 8, we use the same dynamic transmission pattern as in Section 5.5.2 and present the resulting Δ_i and coefficient of variations. We now see that although all Δ_i 's are still positive (meaning that transmitting all ones still results in the highest RO frequency), transmitting all zeros (d_0) has nearly the same behavior. Furthermore, the ordering of the

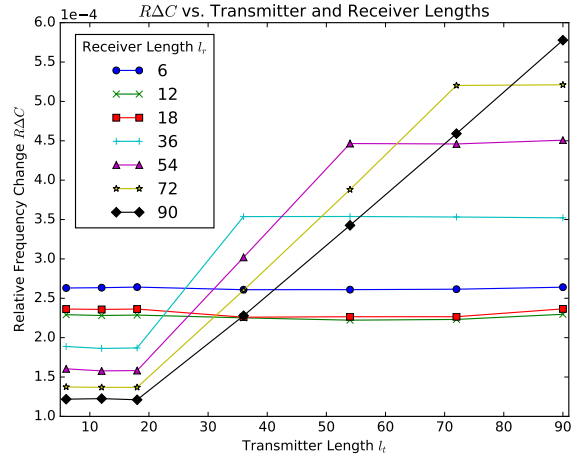


Figure 9: $R\Delta C$ for different length combinations

patterns exactly mirrors their relative switching activity: $0 \approx \Delta_0 < \Delta_1 \approx \Delta_2 \approx \Delta_4 < \Delta_3$. Any patterns in the same switching activity group come from the same distribution ($p \geq 0.27$), while any pair with different switching activity differs significantly ($p < 10^{-24}$).

As shown in the bottom rows of Table 8, we repeated this experiment, this time filling the space between the top and bottom of the ring (spanning $(x_r, y_r + 1)$ to $(x_r, y_r + 39)$) with $39 * 8 = 312$ LUTs. The results are similar, but the overall magnitude is smaller. This is to be expected since fewer than half the number of buffers are used.

5.6 Length

In this section, we characterize the effect of the lengths of the transmitter and receiver wires by varying l_t and l_r (Figure 5). For these tests we return to the more customary long wire transmitter & receiver setup with a slowly alternating transmission ($n = 21$), as described earlier.

Figure 9 shows the relative change in frequency for different combinations of receiver and transmitter lengths. For clarity we only show the results for device 0, but the other two devices have nearly identical results.

For a given ring oscillator length l_r , there are 3 distinct segments for $R\Delta C$ as the transmitter length l_t increases. The first segment occurs for $l_t \in \{6, 12, 18\}$, corresponding to transmitters in which the top and bottom buffers are separated by a vertical distance smaller than the full length of a VLONG. We see that $R\Delta C$ remains constant over this span, which is to be expected since, electrically, the entire VLONG is driven even if the output tap does not take full advantage of the length.

The second segment is the region where $l_t \leq l_r$. Here, $R\Delta C$ increases linearly with l_t , suggesting that the phenomenon roughly affects the delay of each VLONG equally.

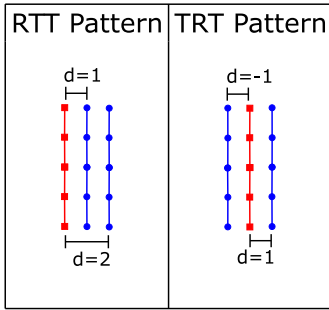


Figure 10: Relative placement of multiple transmitters (blue dots) compared to the receiver (red squares)

The final region consists of $l_t > l_r$, where RAC remains constant. This occurs because there is no overlap between the newly added segments of the transmitter and the ring oscillator receiver.

We can also identify the effect of a given transmitter length l_t on receivers of different lengths l_r . Among receivers with $l_r \geq l_t$, a smaller l_r results in a larger effect. This is because the transmitter affects only the first l_t VLONGs, which represent a larger portion of total delay in smaller ROs.

The opposite is true when $l_r \leq l_t$: the larger the RO, the bigger the resulting effect. We believe this is because although delay of the routing scales linearly, the delay associated with the inverter and buffer LUTs remains constant. Thus, the routing delay represents a larger fraction of the overall delay for larger ROs. Since this phenomenon only seems to act on routing delay, larger ROs are affected more than shorter ones.

5.7 Multiple Transmitters

In this section, we investigate the received effect when using multiple transmitters, T_0 and T_1 . In this experiment each transmitter and the receiver use two VLONG segments ($l_t = l_r = 36$). As seen in Figure 6 (*Transmitter 0* and *Transmitter 1*), the transmitters are driven independently and cycle through all 2-bit combinations over multiple sampling periods. As seen in Figure 10, two different transmitter arrangements are tested. In the first, both transmitters are on the same side of the receiver (RTT, where T_0 is at a distance $d = 2$, and T_1 at a distance $d = 1$). In the second test, the receiver is between the transmitters (TRT, where T_0 is at a distance $d = -1$, and T_1 at a distance $d = 1$).

Figure 11 shows the ring oscillator counts for the RTT experiment. Here, the RO counts appear to only be affected by the value of the closer transmitting wire, T_1 . There is a clear distinction between $T_1 = 0$ and $T_1 = 1$ ($p < 10^{-145}$) while the data is statistically indistinguishable with regards to T_0 ($p > 0.17$). Despite our findings in Section 5.3.1, where a transmitter at $d = 2$ is able to

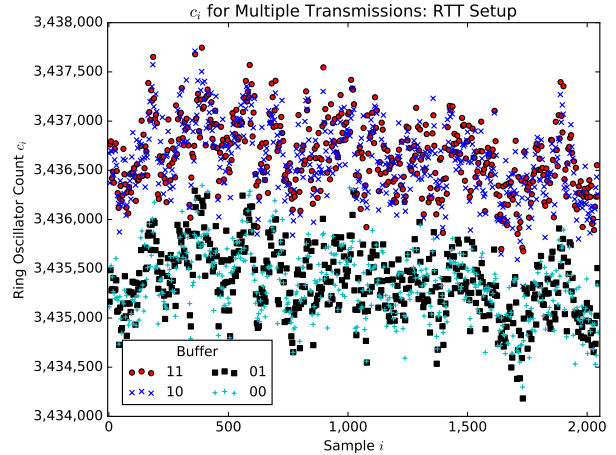


Figure 11: Sensing two transmitters using the RTT setup

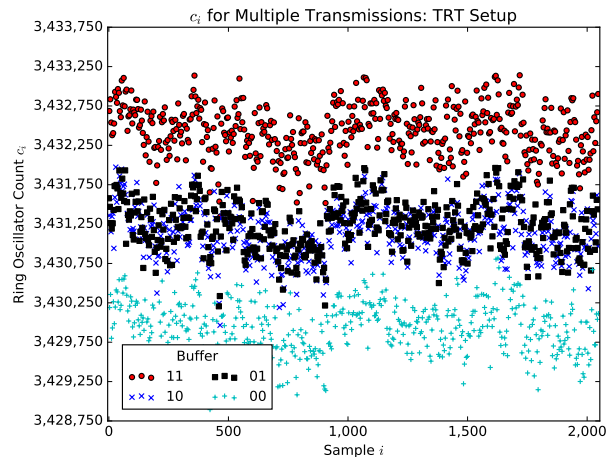


Figure 12: Sensing two transmitters using the TRT setup

impact the receiver, the effects of the closer transmitting wire appear to overwhelm the influence of the further transmitter.

Figure 12 shows the ring oscillator counts for the TRT experiment. As we would expect, T_0 and T_1 have roughly equal influence on the RO. The counts are highest when both transmitters are one, lowest when they are both zero, and in-between otherwise. Although even the difference between (0, 1) and (1, 0) is statistically significant ($p < 10^{-3}$, compared to $p < 10^{-189}$) due to small asymmetries in routing, the data appears too noisy to be practically distinguished. We discuss possibilities for this in Section 6.

5.8 Further Experiments

Although due to space considerations we limited our discussion thus far to vertical wires, we have verified that

6 Discussion

As mentioned earlier, the phenomenon discussed in this paper can be intentionally leveraged by FPGA application developers. For example, its use as a no-contact debugging tap eliminates fan-out load for critical signals and may make it easier to incrementally add or remove debugging logic. Similarly, this phenomenon could be used to check an IP watermark with minimal impact or, flipping the transmitter and receiver, as a protection scheme to unlock IP capabilities in the field.

At the same time, the risk for unintentionally leaking secrets also exists. Modern IP blocks can be quite large, which makes routing through monolithic black-box IP a necessity. The high level of integration required to build complex systems is precisely why modern FPGA tool-suites support IP block route-through.

No matter if the interaction between long wires that we have described here is used in a constructive manner to add new capabilities or in a malicious manner to steal secrets, FPGA design tools will need to be aware of the phenomenon. For example, developers may need some method to denote when wires carry information that should or should not be shared. Similarly, routing tools will need to account for the capabilities or risk associated with using long wires in the same routing channel. We may also require new tools for design rule checks to identify or enforce routing proximity. Knowledge of this phenomenon may also have implications for placement tools.

This phenomenon also has implications for a variety of applications that rely on ring oscillators. For example, the ROs in True Random Number Generators (TRNGs) or Physically Unclonable Functions (PUFs) can be manipulated by the observed behavior. Thus, it may be important to pack as much of this logic as possible into a single CLB, eliminating the use of external routing.

In terms of mitigating this effect, FPGA application designers can protect sensitive signals by intentionally occupying adjacent wires, minimizing the possibility for undue external manipulation or detection. Furthermore, the physical design of the FPGAs themselves, both at the architecture and the transistor level likely have a role to play.

While we have characterized many aspects of this phenomenon, there are others we would like to investigate in the future. For example, both the utility and risk associated with this behavior hinges upon its use as a communication medium. Thus, we would like to characterize the potential bandwidth and possible encoding schemes that can be used. Similarly, further characterization of noise and multi-transmitter/multi-receiver issues is important. Finally, a mechanism for synchronizing the transmitter and receiver may improve bandwidth.

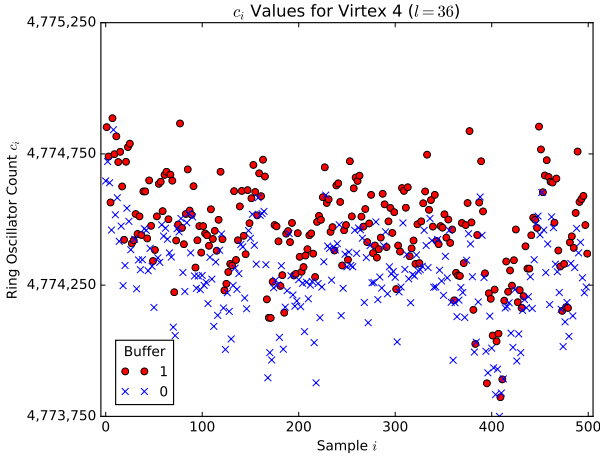


Figure 13: RO counts for Virtex 4 with $l = 36$

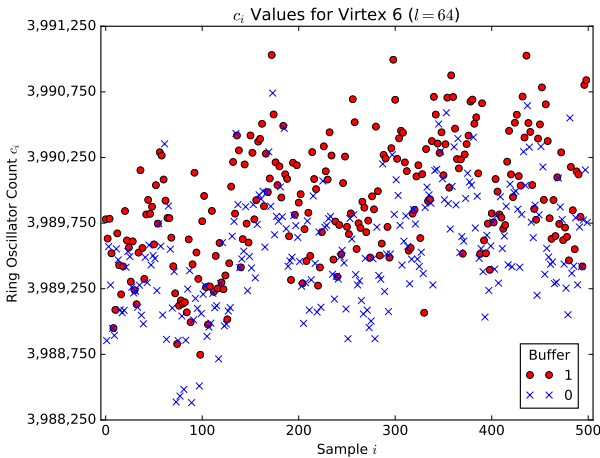


Figure 14: RO counts for Virtex 6 with $l = 64$

the phenomenon also occurs for horizontal HLONGs. We also confirmed that different RO types can be used: multiple inverters (rather than one inverter and multiple buffers) and different numbers of stages all detect this phenomenon. Based on the results in Section 5.6, we suspect that maximizing the fraction of routing delay as a proportion of the overall delay (by reducing the number of LUT stages) would help increase the sensitivity. We leave this as future work.

Finally, we also ran some early tests on Virtex 4 (Figure 13) and Virtex 6 (Figure 14) devices. Though the phenomenon is still present, the correlation appears to be an order of magnitude smaller than for the Virtex 5. Additional future experiments are needed to determine appropriate parameters for less noisy results.

7 Conclusions

In this paper, we have demonstrated that the value carried by a long wire influences the delay of neighboring long wires. This effect is small, but measurable and surprisingly resilient. Specifically, when a long wire carries a one, the delay observed by neighboring wires is reduced.

We have shown that this interaction between long wires can be detected with very small circuits – the most basic system relies on only 5 LUTs to implement both the transmitter and receiver. Although we have made no attempt to determine the precise electrical or magnetic mechanism that causes this behavior, we have thoroughly characterized the phenomenon in terms of when it will occur and how strongly it will present itself.

We show that the behavior is present in multiple different Virtex 5 devices and can be implemented in a variety of arrangements, including different locations, different orientations of the transmitter and receiver, and with competing transmitting circuits. Furthermore, early results suggest the phenomenon occurs in both earlier and more recent device families. We also demonstrate that the phenomenon dominates a competing effect caused by switching activity.

We have also discussed and evaluated techniques for classifying the received data both experimentally and analytically, reaching over 95% classification accuracy over a range of different transmitted signals, including those that persist for as little as $82\mu s$.

The observed behavior has the potential to be used for no-contact communication and may unlock new capabilities for FPGA application designers. This also has implications for the correctness and security of FPGA-based circuits.

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